WHAT IS CLAIMED IS:

1. A memory card comprising:

a plurality of external terminals;

an interface unit; and

an erasable and writable nonvolatile memory,

wherein said plurality of external terminals include a select terminal coupled to a pull-up resistor, and

wherein said interface unit selects a relatively low resistance value for the pull-up resistor of said select terminal before performing mode determination for the memory card based on an input from said select terminal, and selects a relatively high resistance value after said mode determination.

2. A memory card according to claim 1, wherein said mode determination for the memory card is performed in response to reception of an initialization command to the memory card.

3. A memory card according to claim 1, wherein, when said mode determination is performed, said interface unit sets an interface mode with an outside to a first operating mode in response to a HIGH level of said select terminal, and sets the interface mode with the outside to a second operating mode in response to a LOW level of said select terminal.

4. A memory card according to claim 3, wherein said memory card is based on a standard of Multimedia Card, said first operating mode is an SPI mode, and said second operating mode is an MMC mode.

5. A memory card according to claim 1, wherein said selection of the low resistance value is performed stepwise and the stepwise selection assumes that a lower resistance value is selected earlier.

6. A memory card according to claim 1,

wherein said plurality of external terminals include a data terminal coupling to a pull-up resistor, and

wherein said interface unit selects a relatively low resistance value for the pull-up resistor of said data terminal during a period after a write command until a start bit of data to be written which is supplied to said data terminal is detected and selects a relatively high initial resistance value after said detection of the start bit.

7. A memory card comprising:

a plurality of external terminals; and

an internal circuit having erasable and writable nonvolatile storing means,

wherein said internal circuit lowers, in performing mode determination in response to an initialization command and based on an input from a select terminal as one of said external terminals, a resistance value of a pull-up resistor of said select terminal before a determination timing and restores the pull-up resistor to an initial resistance value after said mode determination.

8. A memory card comprising:

a plurality of external terminals; and

an internal circuit having erasable and writable nonvolatile storing means,

wherein said internal circuit lowers, during a period after receiving a write command until receiving of a start bit of data to be written which is supplied to a data terminal as one of said external terminals is detected, a resistance value of a pull-up resistor of said data terminal and restores the pull-up resistor to an initial value after said detection of the start bit.

9. An electronic device comprising:

a plurality of external terminals; and

an internal circuit,

wherein said internal circuit relatively lowers, in performing mode determination in response to an initialization command and based on an input from a select terminal as one of said external terminals, an input impedance of said select terminal before a determination timing and returns the input impedance to an initial value after said mode determination.

10. An electronic device comprising:

a plurality of external terminals; and

an internal circuit,

wherein said internal circuit relatively lowers, during a period after receiving a write command until receiving of start bit of data to be written which is supplied to a data terminal as one of said external terminals is detected, an input impedance of said data terminal, and returns the input impedance to an

initial value after said detection of the start bit.